IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A semiconductor die, comprising:
a semiconductor substrate having a front side and a back side;
an integrated circuit on a portion of said front side;
a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate; and
a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit.

2. (Original) A semiconductor die in accordance with claim 1, wherein said stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

3. (Original) A semiconductor die in accordance with claim 1, wherein said stress-balancing layer comprises an adhesive material.

4. (Original) A semiconductor die in accordance with claim 1, wherein said stress-balancing layer comprises a layer for laser-marking.

5. (Original) A semiconductor die in accordance with claim 1, further comprising an adhesive layer attached to said stress-balancing layer.

6. (Original) A nonwarp semiconductor die in accordance with claim 5, wherein said adhesive layer comprises a layer of material for laser-marking.

7. (Original) A nonwarp semiconductor die, comprising:

a semiconductor substrate having a front side, a back side, and a low ratio of height to a horizontal dimension;

an integrated circuit on said front side;

a passivation layer covering a portion of said integrated circuit exerting a stress on said substrate front side; and

a stress-balancing layer covering at least a portion of said back side, said stress-balancing layer for balancing a portion of said front side stress with a generally equivalent back side stress.

8. (Original) A nonwarp semiconductor die in accordance with claim 7, wherein said stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

9. (Original) A nonwarp semiconductor die in accordance with claim 7, wherein said stress-balancing layer comprises an adhesive material.

10. (Original) A nonwarp semiconductor die in accordance with claim 9, wherein said stress-balancing layer comprises a layer of material for laser-marking.

11. (Original) A nonwarp semiconductor die in accordance with claim 7, further comprising an adhesive layer attached to said stress-balancing layer.

12. (Original) A nonwarp semiconductor die in accordance with claim 11, wherein said adhesive layer for laser-marking comprises a layer of material for laser-marking.

13. (Currently Amended) A semiconductor die, comprising:

a semiconductor substrate having a front side having an integrated circuit on a portion thereof and a back side;

a passivation layer covering a portion of said integrated circuit causing a stress on at least a portion of the semiconductor substrate; and

a stress-balancing layer covering at least a portion of said back side substantially balancing the stress caused by the front side passivation layer covering a portion of said integrated circuit.

14. (Original) The semiconductor die of claim 13, wherein said stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

15. (Original) The semiconductor die of claim 13, wherein said stress-balancing layer comprises an adhesive material.

16. (Original) The semiconductor die of claim 13, wherein said stress-balancing layer comprises a layer for laser-marking.

17. (Original) The semiconductor die of claim 13, further comprising an adhesive layer attached to said stress-balancing layer.

18. (Original) The semiconductor die of claim 17, wherein said adhesive layer comprises a layer of material for laser-marking.

19. (Original) A reduced stress semiconductor die, comprising:

a semiconductor substrate having a front side, a back side, and a low ratio of the height of the semiconductor substrate to a horizontal dimension of the semiconductor substrate;

an integrated circuit on said front side of the semiconductor substrate;

a passivation layer covering a portion of said integrated circuit causing a force acting on a portion of said substrate front side; and

a force-balancing layer covering at least a portion of said back side, said force-balancing layer for balancing a portion of said force on said front side.

20. (Original) The semiconductor die of claim 19, wherein said force-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

21. (Original) The semiconductor die of claim 19, wherein said stress-balancing layer comprises an adhesive material.

22. (Original) The semiconductor die of claim 21, wherein said stress-balancing layer comprises a layer of material for laser-marking.

23. (Original) The semiconductor die of claim 19, further comprising an adhesive layer attached to said stress-balancing layer.

24. (Original) The semiconductor die of claim 23, wherein said adhesive layer for laser-marking comprises a layer of material for laser-marking.